REMARKS

Claims 1-53 are pending in the application. Claims 1, 18, 35 and 53 are rejected under 35 U.S.C. 102(b) as being deemed anticipated by U.S. Patent No. 4,607,325 (Horn). Claims 1, 18, 35 and 53 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,178,542 (Dave). Claims 1-12, 15, 18-29, 32, 35-46, 49, 52 and 53 are rejected under 35 U.S.C. 102(e) as being anticipated by Jevtic et al. (U.S. Patent No. 6,519,498). Claims 13, 14, 16, 17, 30, 31, 33, 34, 47 48, 50 and 51 are rejected under U.S.C. 103(a) as being deemed unpatentable over Jevtic et al. (U.S. Patent No. 6,519,498) as applied to claims 1, 15, 18, 32, 35 and 49 above, in view of Dave (U.S. Patent No. 6,178,542). Of the claims, claims 1, 18, 35, 52 and 53 are independent. The application, as argued herein, is believed to overcome the rejections.

Regarding Objections to the Specification

The specification has been objected to because subject matter in pending applications has been incorporated by reference to an Attorney Docket Number. In response, the specification has been amended to include the U.S. Application Serial Number assigned to the Attorney Docket Number.

Reconsideration of the objection to the specification is respectfully requested.

Regarding Rejections under 35 U.S.C. 112

Claims 1-53 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In response, claims 1, 4-6, 9, 11-13, 15-18, 22, 25, 28-29, 32-35, 39, 42, 45, 46, 48-53 have been amended to provide antecedent basis.

Claims 11 and 12 have been amended to clarify that the cost is updated based on the stored schedule execution costs with more recent schedule execution costs being more important; that is, the importance of stored schedule execution costs decreases with time. (*See* Page 22, lines 16-22.)

Reconsideration of the rejections under 35 U.S.C. 112 is respectfully requested.

Regarding Rejections under 35 U.S.C. 102(b)

Claims 1, 18, 35 and 53 are rejected under 35 U.S.C. 102(b) as being deemed anticipated by U.S. Patent No. 4,607,325 (Horn).

The Applicants' claimed invention is directed to scheduling tasks in a constrained dynamic application; that is, a schedule for a program for a computer. A set of static schedules is defined for the application based on scheduling states. Each static schedule includes an assignment of tasks to processors. During run time, a cost of a set of static schedules based on performance of the application is learned and a static schedule with a lowest cost is designated as an optimal schedule for a scheduling state. (*See* Page 8, lines 1-3, Page 5, lines 18-19 in the Applicants' specification as originally filed.)

Cited prior art, Horn is directed to a computer that controls a process for a power plant. The computer determines which of the components (boiler, turbines, fuel/water pumps) should be running/idle so that the power demands for electric power are met while the total cost of the purchased power and fuels is minimized. The computer takes into consideration the cost of starting up and shutting down components in the power plant.

Horn's discussion of a computer for controlling operating status of components in a power plant does not teach or suggest at least the applicants' claimed "defining a set of static schedules or tasks in an application, each static schedule including an assignment of tasks to processors." In contrast, Horn merely discusses monitoring the components in order to determine which to change a component status from run to idle and idle to run. Furthermore, the cited art does not teach or suggest the Applicants' claimed "during run time, learning the cost of a set of static schedules based on performance of the application". In contrast, the cost of running the power plant is not learned during run time, instead the cost of running individual components in the power plant (fuel for boiler, electric power for pumps and the cost for changing idle/run status of a component) is already known and used to determine which components should be set to run or idle. (*See* Col. 6,line 58 – Col. 7, line 2; Col. 8, line 10 – 37.)

Independent Claim 18 recites a like distinction in terms of an apparatus and thus similarly patentably distinguishes over the prior art. Independent Claims 35 and 53 include like limitations distinguishing over the cited art.

As such the § 102(b) rejection of Claims 1, 18, 35 and 53 is believed to be overcome.

Regarding Rejections under 35 U.S.C. 102(e)

Claims 1, 18, 35 and 53 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,178,542 (Dave).

Cited prior art Dave is directed to deriving architecture of an embedded system from a task graph using hardware-software co-synthesis (simultaneous synthesis of the hardware and software architectures). (*See* Col. 4, lines 17-20 and Abstract.)

Dave does not teach or suggest at least the Applicants' claimed "based on scheduling states, defining a set of static schedules for an application, each static schedule including an assignment of tasks to processors". In contrast, Dave merely discusses use of a task graph to derive an architecture for an embedded system from a task graph. (*See* Col. 13, lines 40-66.)

Independent Claim 18 recites a like distinction in terms of an apparatus and thus similarly patentably distinguishes over the prior art. Independent Claims 35 and 53 include like limitations distinguishing over the cited art.

As such the § 102(e) rejection of Claims 1, 18, 35 and 53 is believed to be overcome.

Claims 1-12, 15, 18-29, 32, 35-46, 49, 52 and 53 are rejected under 35 U.S.C. 102(e) as being anticipated by Jevtic et al. (U.S. Patent No. 6,519,498).

Cited prior art, Jevtic is directed to scheduling of wafer processing in a multi-chamber semiconductor wafer processing tool. All possible schedules are generated and analyzed to determine a schedule that produces the highest throughput. Prior to run time, the schedule with the highest throughput is deemed optimal and is downloaded to the sequencer. (*See* Col. 14, lines 57-64.)

Jevtic does not teach or suggest the Applicants' claimed "based on scheduling states, defining a set of static schedules for the application." In contrast, Jevtic merely discusses a multi chamber semiconductor wafer processing tool with a single state, that is, a given processing sequence (order in which processes are applied to a wafer) and tool configuration (physical placement of the chambers). A process can be performed in more than one chamber, there can be more than one processing sequence for the tool configuration. Only the optimal

processing sequence generated during simulation is used by the tool. (*See* Col. 5, lines 32-53 and Col6, lines 31-61.)

Additionally, Jevtic does not teach or suggest the Applicants' claimed "static schedule including an assignment of tasks to processors". In contrast, Jevtic's schedule is based on a trace which maps a process sequence into a set of chambers with each chamber dedicated to a process.

Furthermore, Jevtic does not teach or suggest the Applicants' claimed "during run-time, based on the scheduling state, learning a cost of a set of static schedules based on performance of the application." In contrast, Jevtic discusses selecting an optimal schedule prior to run-time. A schedule is selected based on throughput computed on a tool simulator. Only the selected optimal schedule is downloaded to the sequencer. With all traces generated based on a single scheduling state, there is no suggestion of learning a cost of a set of static schedules based on performance of the application as claimed in base claim 1.

Independent Claim 18 recites a like distinction in terms of an apparatus and thus similarly patentably distinguishes over the prior art. Independent Claims 35 and 53 include like limitations distinguishing over the cited art. Claims 1-12 and 15 are dependent on Claim 1, Claims 19-29 and 32 are dependent on Claim 18. Claims 36-46, 49, and 52 are dependent on Claim 35.

As such the § 102(e) rejection of Claims 1-12, 15, 18-29, 32, 35-46, 49, 52 and 53 is believed to be overcome.

Regarding Rejections under 35 U.S.C. 103(a)

Claims 13, 14, 16, 17, 30, 31, 33, 34, 47 48, 50 and 51 are rejected under U.S.C. 103(a) as being deemed unpatentable over Jevtic et al. (U.S. Patent No. 6,519,498) as applied to claims 1, 15, 18, 32, 35 and 49 above, in view of Dave (U.S. Patent No. 6,178,542).

One of ordinary skill in the art of scheduling tasks in an application would not look to methods of scheduling wafer processing in a multi-chamber semiconductor wafer processing tool, or to methods of deriving an architecture for an embedded system to provide a scheduling system for scheduling tasks in an application.

Claims 13, 14, 16, and 17 are dependent on Claim 1, Claims 30, 31, 33, and 34 are dependent on Claim 18, Claims 47, 48, 50 and 51 are dependent on Claim 35. Thus, claims 13,

14, 16, 17, 30, 31, 33, 34, 47 48, 50 and 51 are non-obvious over the cited prior art for the same reasons already discussed for independent claims 1, 18, 35 and 53

Thus, none of the cited art alone or in combination teaches or suggests the applicants' claimed invention. Accordingly, the present invention as now claimed is not believed to be anticipated or made obvious by the cited art or any of the prior art. In view of the foregoing, reconsideration of the rejections under 35 U.S.C. § 102(e), 35 U.S.C. § 102(b) and 35 U.S.C. § 103(a) is respectfully requested.

Regarding new Claim 54

Support for new added Claim 54 is found at least on page 13, lines 26-28. No new matter is introduced. New Claim 54 is dependent on Claim 1, thus the forgoing arguments and distinctions over the prior art apply. Acceptance is respectfully requested.

Supplemental Information Disclosure Statement

A Supplemental Information Disclosure Statement (SIDS) is being filed concurrently herewith. Entry of the SIDS is respectfully requested.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,
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